CLAIMS:

1. A linear RF transmitter for the transmission of non-constant envelope modulated signals, comprising:

Amplitude baseband processing means arranged to resolve an input signal into amplitude & phase components, and to further resolve the phase components into In-phase (I) and quadrature (Q) components;

conversion means arranged to generate analogue representations of the signal components;

phase modulation means arranged to receive the analogue representations of the In-phase and quadrature components and to upconvert and phase modulate the I and Q components into an RF signal;

output power amplifier means arranged to receive the phase modulated RF signal and amplify the signal for transmission;

direct amplitude modulation means arranged to receive an amplitude component of the input signal and to control the output power amplifier means in accordance with the amplitude component whereby to amplitude modulate the RF signal; and

synchronising means arranged to monitor the RF signal and control the amplitude component conversion means in response to the RF signal.

Cancel ~~2.~~ A transmitter according to claim 1 wherein the baseband processing means are further arranged to resolve the amplitude component from the input signal, and the conversion means are further arranged to generate an analogue representation of the amplitude component and feed the analogue representation to the direct amplitude modulating means.

3. A transmitter according to claim ~~2~~ 1 wherein the phase modulation

means further comprise:

a first oscillator arranged to produce an intermediate frequency signal;

a first IQ modulator means to phase modulate the intermediate frequency signal with the I and Q signal components;

a second oscillator arranged to produce a reference frequency signal; and

a phase lock loop to upconvert the modulated intermediate frequency signal to the radio frequency; wherein

the upconverted intermediate frequency signal is output as the phase modulated RF signal at a frequency the sum of the intermediate frequency and the reference frequency.

4. A transmitter according to claim 1, wherein the phase modulation means further comprise:

a first oscillator arranged to produce an intermediate frequency signal;

a first IQ modulator means to phase modulate the intermediate frequency signal with the I and Q signal components;

an envelope detector means to detect the amplitude component of the phase modulated intermediate frequency signal feed the amplitude component to the direct amplitude modulation means;

limiting means to remove the amplitude component from the phase modulated intermediate frequency signal;

a second oscillator arranged to produce a reference signal; and

a phase lock loop arranged to receive the limited phase modulated intermediate frequency signal and to upconvert said signal to the radio frequency;

wherein the upconverted intermediate frequency signal is output as the phase modulated RF signal at a frequency the sum of the intermediate frequency and the reference frequency.

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5. A transmitter according to claim 3 or 4, wherein the phase lock loop comprises:

a voltage controlled oscillator;

phase comparison means; and

summing and mixing means,

wherein the phase comparison means is arranged to receive the phase modulated intermediate frequency signal and a mixed signal output from the mixer means and to control the voltage controlled oscillator therefrom, and wherein the voltage controlled oscillator is arranged to output a constant amplitude phase modulated signal in response to the phase comparison means and wherein the summing and mixing means are arranged to sum the constant amplitude phase modulated signal with the RF signal fed back from the output of the output power amplifier means, and mix the resulting signal with the reference frequency signal to generate the mixed signal fed to the phase comparison means.

6. A transmitter according to claims 3 to 5, wherein the phase modulation means further comprise:

binary modulator means arranged to receive the phase modulated RF signal and to be controlled by the baseband processing means to remove any 180 degree phase shifts introduced into the phase modulated RF signal.

7. A transmitter according to claims 3 to 5, wherein the phase modulation means further comprise:

a second IQ modulator means arranged to receive the phase modulated RF signal and the baseband I and Q components and to further phase modulate the phase modulated RF signal with the baseband I and Q components whereby to remove any unwanted phase modulation introduced into the phase modulated RF signal.

8. A transmitter according to claim 7 wherein the second IQ modulator means are incorporated within the phase lock loop.

9. A transmitter according to claim 7, wherein both first and second IQ modulator means are incorporated in the feedback path of the PLL.

10. A transmitter according to claims 7 to 9, and further comprising phase modulation synchronising means; and

respective in-phase and quadrature signal component delay means arranged to control the phase modulation performed in the second IQ modulation means;

wherein said phase modulation synchronising means is arranged to detect phase modulation errors introduced into the phase modulated RF signal and to control the delay means therefrom whereby to reduce modulation synchronisation errors in the phase modulated RF signal.

11. A transmitter according to claim 10, wherein the phase modulation synchronising means is arranged to receive the amplitude component of the input signal, a phase rotation signal from the baseband processing means, and the voltage controlled oscillator control signal from the phase comparison means, and to detect phase modulation errors therefrom.

12. A transmitter according to claim 5 wherein the phase lock loop further comprises:

summing means disposed between the phase comparison means and the voltage controlled oscillator;

differentiation means arranged to receive the baseband component from the baseband processing means and to differentiate the phase component with respect to time,

wherein the summing means receives the differentiated phase component and the output from the phase comparison means and steers the voltage controlled oscillator on the basis of the resulting sum.

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claim 1

13. A transmitter according to any of the preceding claims wherein the conversion means further comprises:

a separate digital to analogue converter for each of the amplitude component, the In-phase component and the quadrature component of the input signal;

clock means for supplying a clock signal to each of the digital to analogue converters; and

conversion control means for controlling the conversion in response to a synchronising control signal from the synchronising means.

14. A transmitter according to claim 13, wherein the conversion control means is a delay circuit arranged to delay the clock signal fed to the digital to analogue converters, whereby to control at least the phase of the generated representations of the input signal components.

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15. A transmitter according to claims 13 and 14, wherein the conversion means further comprises:

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a separate analogue interpolation filter for each of the amplitude component, the In-phase component, and the quadrature component of the input signal, each filter being arranged to receive the respective analogue representations of each input signal component.

claim 1

16. A transmitter according to ~~any of the preceding claims~~ wherein the direct amplitude modulation means further includes power economy means.

17. A transmitter according to claim 16, wherein the power economy means comprise:

a first power supply arranged to supply power at a first supply voltage to a first conducting device;

a second power supply arranged to supply power at a second supply voltage to a second conducting device; and

switching means arranged to switch between the first and second conducting devices;

wherein the second supply voltage is higher than the first supply voltage, and the switching means is arranged to switch from the first conducting device to the second conducting device when an amplitude peak occurs in the amplitude component of the input signal.

18. A transmitter according to claim 17, wherein the first and second power supplies are each switched mode power supplies.

19. A transmitter according to claim 16, wherein the power economy means comprise:

a switching device arranged to be controlled by the baseband

processing means; and

an inductor connected between the power amplifier and the switching device;

wherein the baseband processing means controls the switching device to create a voltage pulse which is integrated by the inductor to give an approximate shape representation of the amplitude component of the input signal.

20. A transmitter according to claim 19, wherein the power economy further comprise:

a comparator amplifier arranged to operate in a linear manner and arranged to receive the amplitude component of the input signal and the integrated voltage pulse, and output a difference signal therefrom; and

an adder arranged to receive the integrated voltage pulse and the difference signal and output a sum signal to the power amplifier corresponding to the sum of the two received signals;

whereby the shape of the voltage pulse may be finely controlled so as to accurately represent the amplitude component of the input signal.

21. A transmitter according any of ~~the preceding claims~~ claim 1, wherein the synchronising means further comprise:

phase detector means arranged to detect the phase of the RF output signal;

amplitude detector means arranged to detect the amplitude envelope of the RF output signal;

synchronisation detector means arranged to detect the synchronisation between the phase and the amplitude of the RF output signal; and

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synchronisation control means arranged to control the conversion means on the basis of the detected synchronisation.

22. A transmitter according to claim 21, wherein the phase detector means further comprises:

a delay circuit and a mixer arranged to act together as an FM discriminator;

a first low pass filter arranged to receive the output of the FM discriminator;

a second low pass filter arranged to receive the output of the FM discriminator; and

a comparator arranged to receive an output from the first low pass filter and compare this with a reference voltage, the difference being used to control the delay circuit so that the FM discriminator outputs a fixed DC level voltage;

wherein the fixed DC voltage is manifested as a voltage pulse at the output of the second low pass filter whenever there is a change of phase.

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23. A transmitter according to claim ~~21~~ CLAIM 21 or 22, wherein an amplitude detector means further comprises:

an envelope detector for detecting the amplitude envelope; and

a differentiator arranged to receive the output of the envelope detector and differentiate the signal with respect to time.

24. A transmitter according to claim 23 wherein the synchronisation detector comprises a sampling gate arranged to sample the differentiated amplitude envelope in response to the voltage pulse from the phase detector whereby when the amplitude and phase of the RF signal are synchronous, the

sampled signal will be zero.